Patent Application Attorney Docket No.: 57941.000041 Client Reference No.: RA208.CIP1.US

APPENDIX D

Receiver circuit 3103 comprises receiver 3116, multiplexer 3119, shift register 3108, and XOR gate 3113. Medium 3102 is coupled to an input of receiver 3116. A receive circuit timing signal is coupled to an input of receiver 3116 at node 3117. A voltage reference signal is coupled to an input of receiver 3116 at node 3118. An output of receiver 3116 is coupled to an input of multiplexer 3119 and to an input of XOR gate 3113. A fill pipe signal is coupled to a selection input of multiplexer 3119 at node 3120. An output of multiplexer 3119 is coupled to a serial data input of shift register 3108. A serial data output of shift register 3108 is coupled to an input of multiplexer 3119 and to an input of XOR gate 3113 via line 3111. An output of XOR gate 3113 provides an error output at node 3114.

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